

In r Patent Application of:
CROCE ET AL.
Serial No. 09/839,596
Filing Date: APRIL 20, 2001

In the Claims:

This listing of claims replaces all prior versions
and listing of claims in the application.

Claims 1-4 (Canceled).

5. (Previously presented) A lateral diffused metal
oxide semiconductor (LDMOS) integrated device comprising:

a semiconductor substrate;

a drain region of a first conductivity type adjacent
said semiconductor substrate and comprising a superficial
buffer region being more heavily doped than adjacent portions
of said drain region;

41 a body region completely surrounded on a bottom and
sides thereof by said buffer region and having a second
conductivity type; and

a source region in said body region and having the
first conductivity type.

6. (Original) The LDMOS integrated device of Claim
5 wherein said drain region has a depth of about 1.5 to 4.5
micrometers.

7. (Original) The LDMOS integrated device of Claim
5 wherein the portions of said drain region adjacent said
superficial buffer region have a dopant concentration of about
 2.5×10^{15} to 2.5×10^{16} atoms cm^{-3} .

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8. (Original) The LDMOS integrated device of Claim 5 wherein said superficial buffer region has a depth of about 0.15 to 0.45 micrometers.

9. (Original) The LDMOS integrated device of Claim 5 wherein said superficial buffer region has a dopant concentration of about 5×10^{16} to 5×10^{17} atoms cm^{-3} .

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10. (Original) The LDMOS integrated device of Claim 5 wherein said body region has a depth of about 0.25 to 0.75 micrometers.

11. (Original) The LDMOS integrated device of Claim 5 wherein said body region has a dopant concentration of about 5×10^{17} to 5×10^{18} atoms cm^{-3} .

12. (Original) The LDMOS integrated device of Claim 5 wherein said drain region is doped with phosphorous; and wherein said body region is doped with boron.

13. (Original) The LDMOS integrated device of Claim 5 wherein said drain region is doped with boron; and wherein said body region is doped with phosphorus.

14. (Previously presented) A lateral diffused metal oxide semiconductor (LDMOS) integrated device comprising:
a semiconductor substrate;
a drain region of a first conductivity type adjacent said semiconductor substrate and comprising a superficial

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buffer region being more heavily doped than adjacent portions of said drain region;

said superficial buffer region having a dopant concentration of about 5×10^{16} to 5×10^{17} atoms cm^{-3} and the adjacent portions of said drain region having a dopant concentration of about 2.5×10^{15} to 2.5×10^{16} atoms cm^{-3} ;

a body region completely surrounded on a bottom and sides thereof by said superficial buffer region and having a second conductivity type; and

a source region in said body region and having the first conductivity type.

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end

15. (Original) The LDMOS integrated device of Claim 14 wherein said drain region has a depth of about 1.5 to 4.5 micrometers.

16. (Original) The LDMOS integrated device of Claim 14 wherein said buffer region has a depth of about 0.15 to 0.45 micrometers.

17. (Original) The LDMOS integrated device of Claim 14 wherein said body region has a depth of about 0.25 to 0.75 micrometers.

18. (Original) The LDMOS integrated device of Claim 14 wherein said body region has a dopant concentration of about 5×10^{17} to 5×10^{18} atoms cm^{-3} .

19-25. (Withdrawn).

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